

# RJK0222DNS

Silicon N Channel Power MOS FET with Schottky Barrier Diode  
High Speed Power Switching

R07DS0125EJ0120

Rev.1.20

May 16, 2012

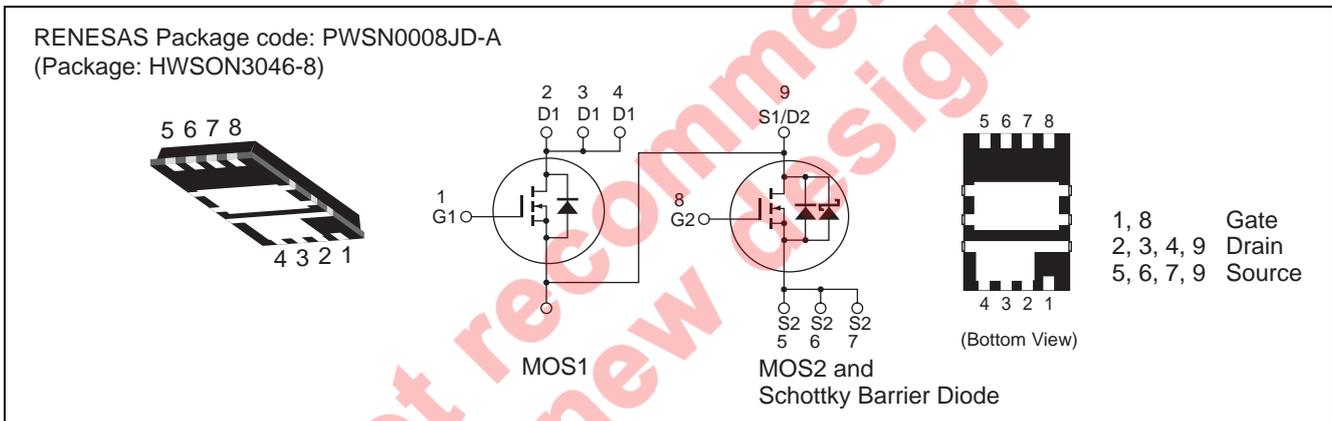
## Application

DC-DC conversion for PC and Server.

## Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- Pb-free
- Halogen-free

## Outline



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		MOS1	MOS2	
Drain to source voltage	V <sub>DSS</sub>	25	25	V
Gate to source voltage	V <sub>GSS</sub>	±20	±12	V
Drain current	I <sub>D</sub>	14	16	A
Drain peak current	I <sub>D(pulse)</sub> <sup>Note 1</sup>	56	64	A
Reverse drain current	I <sub>DR</sub>	14	16	A
Avalanche current	I <sub>AP</sub> <sup>Note 2</sup>	5	8	A
Avalanche energy	E <sub>AS</sub> <sup>Note 2</sup>	3.1	8.0	mJ
Channel dissipation	P <sub>ch</sub> <sup>Note 3</sup>	8	10	W
Channel temperature	T <sub>ch</sub>	150	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
 2. Value at T<sub>ch</sub> = 25°C, R<sub>g</sub> ≥ 50 Ω  
 3. T<sub>c</sub> = 25°C

## Electrical Characteristics

## • MOS1

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	25	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 25 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	7.6	9.2	$\text{m}\Omega$	$I_D = 7 \text{ A}, V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	10.5	13.7	$\text{m}\Omega$	$I_D = 7 \text{ A}, V_{GS} = 4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	—	30	—	S	$I_D = 7 \text{ A}, V_{DS} = 5 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	810	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	130	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	74	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	$R_g$	—	1.2	—	$\Omega$	
Total gate charge	$Q_g$	—	6.2	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	$Q_{gs}$	—	2.8	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	1.9	—	nC	$I_D = 14 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	7	—	ns	$V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}$
Rise time	$t_r$	—	4.1	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	33	—	ns	$R_L = 1.42 \Omega$
Fall time	$t_f$	—	5.1	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	$V_{DF}$	—	0.84	1.10	V	$I_F = 14 \text{ A}, V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	20	—	ns	$I_F = 14 \text{ A}, V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

## • MOS2

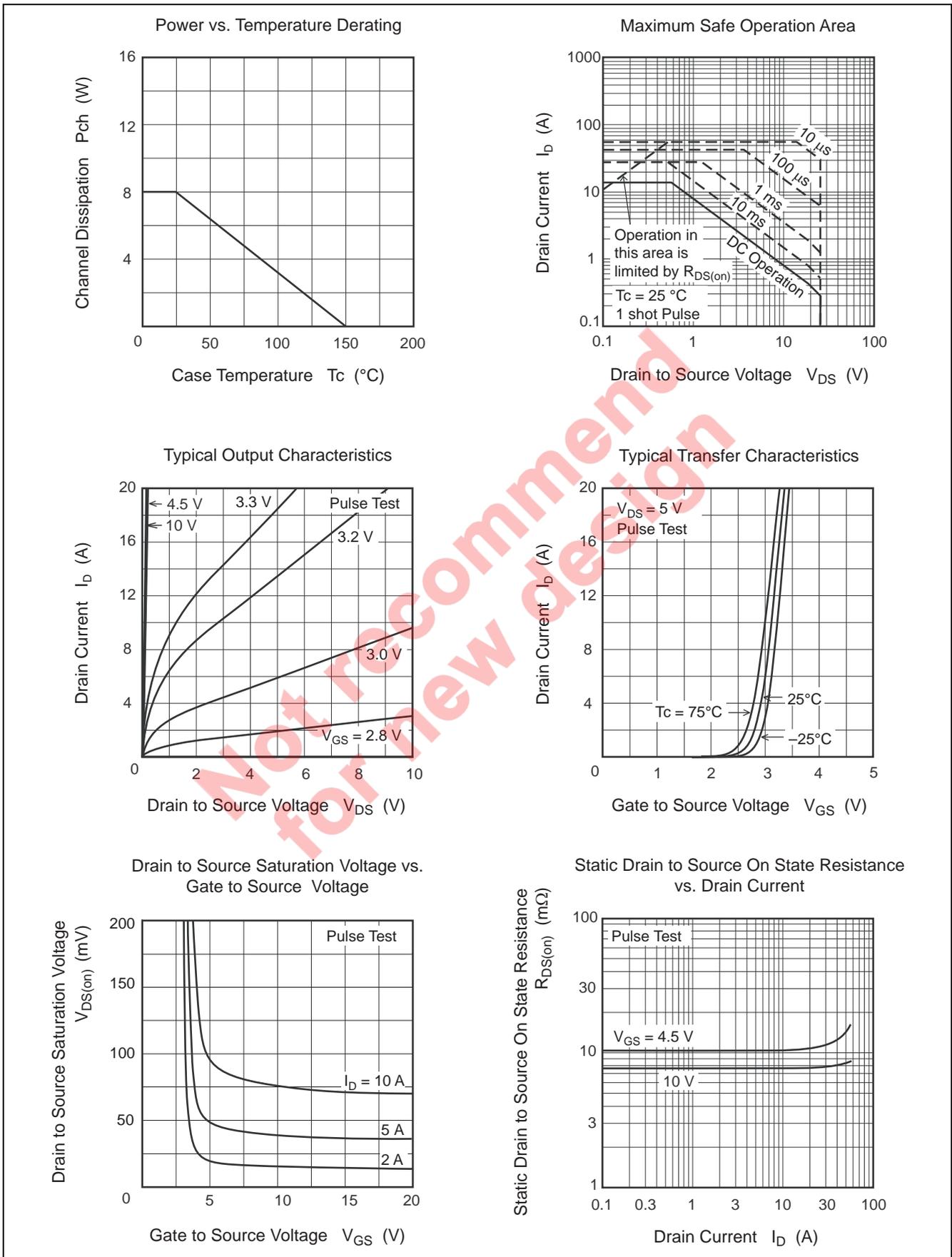
(Ta = 25°C)

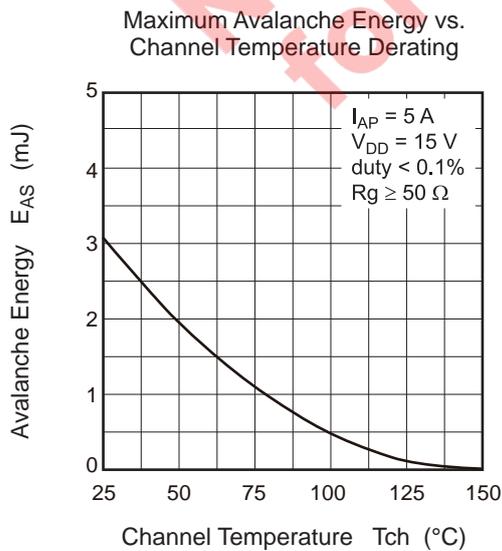
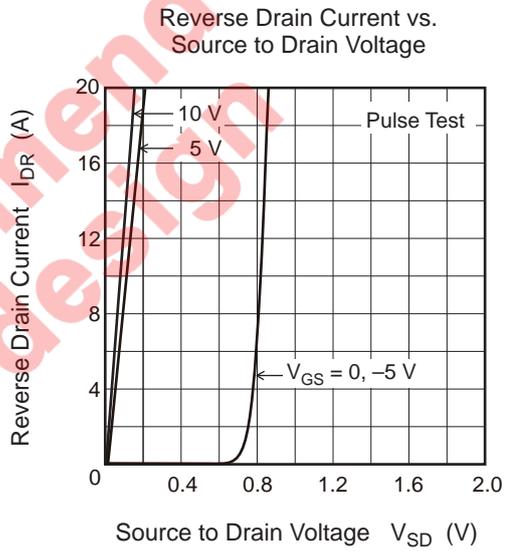
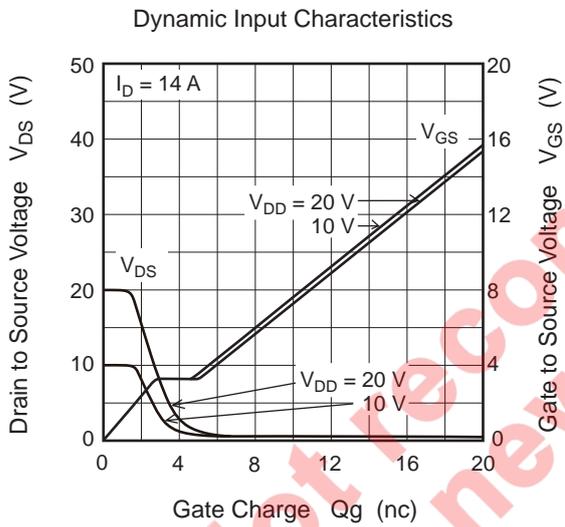
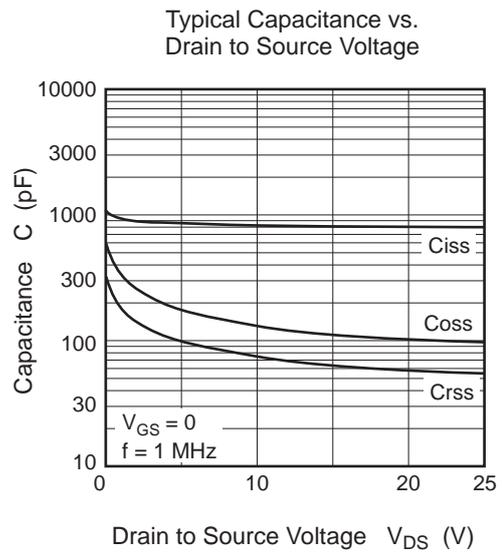
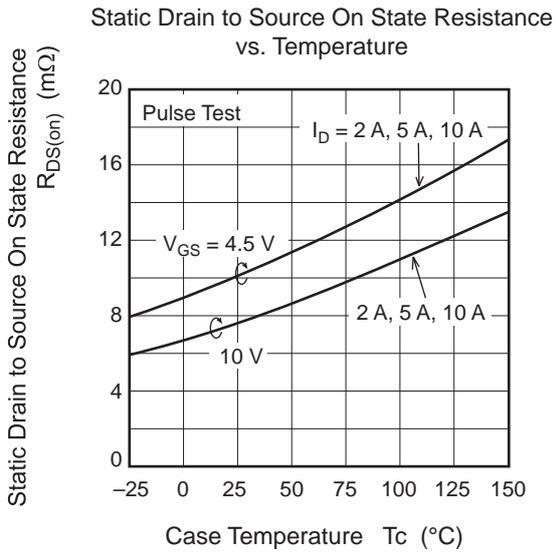
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	25	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	mA	$V_{DS} = 25 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.9	5.9	m $\Omega$	$I_D = 8 \text{ A}, V_{GS} = 8.0 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	6.2	8.1	m $\Omega$	$I_D = 8 \text{ A}, V_{GS} = 4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	—	39	—	S	$I_D = 8 \text{ A}, V_{DS} = 5 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	1680	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	259	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	150	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	$R_g$	—	2.1	—	$\Omega$	
Total gate charge	$Q_g$	—	11.8	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	$Q_{gs}$	—	4.4	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	2.7	—	nC	$I_D = 16 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	9.6	—	ns	$V_{GS} = 8 \text{ V}, I_D = 8 \text{ A}$
Rise time	$t_r$	—	4.2	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	40	—	ns	$R_L = 1.25 \Omega$
Fall time	$t_f$	—	5	—	ns	$R_g = 4.7 \Omega$
Schottky Barrier diode forward voltage	$V_F$	—	0.41	—	V	$I_F = 2 \text{ A}, V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	26	—	ns	$I_F = 16 \text{ A}, V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse

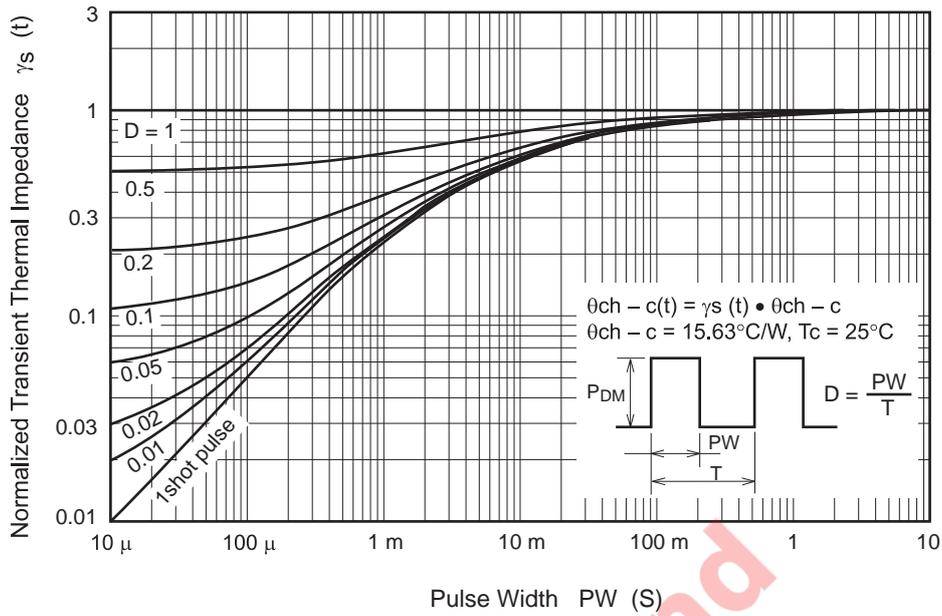
# Main Characteristics

• MOS1

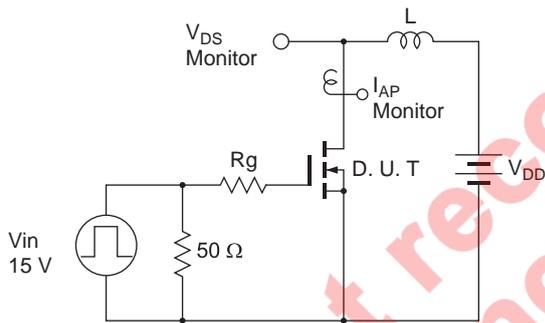




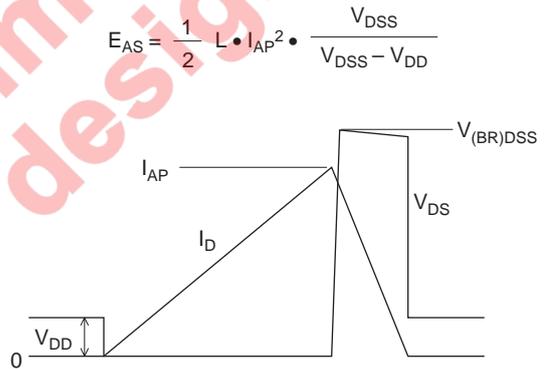
Normalized Transient Thermal Impedance vs. Pulse Width



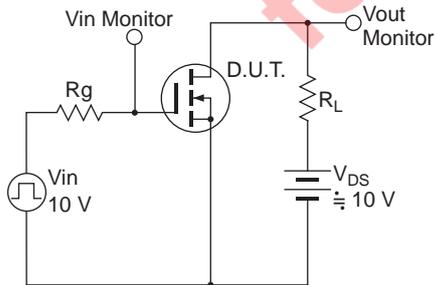
Avalanche Test Circuit



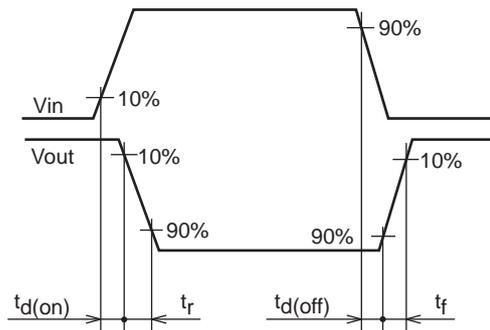
Avalanche Waveform



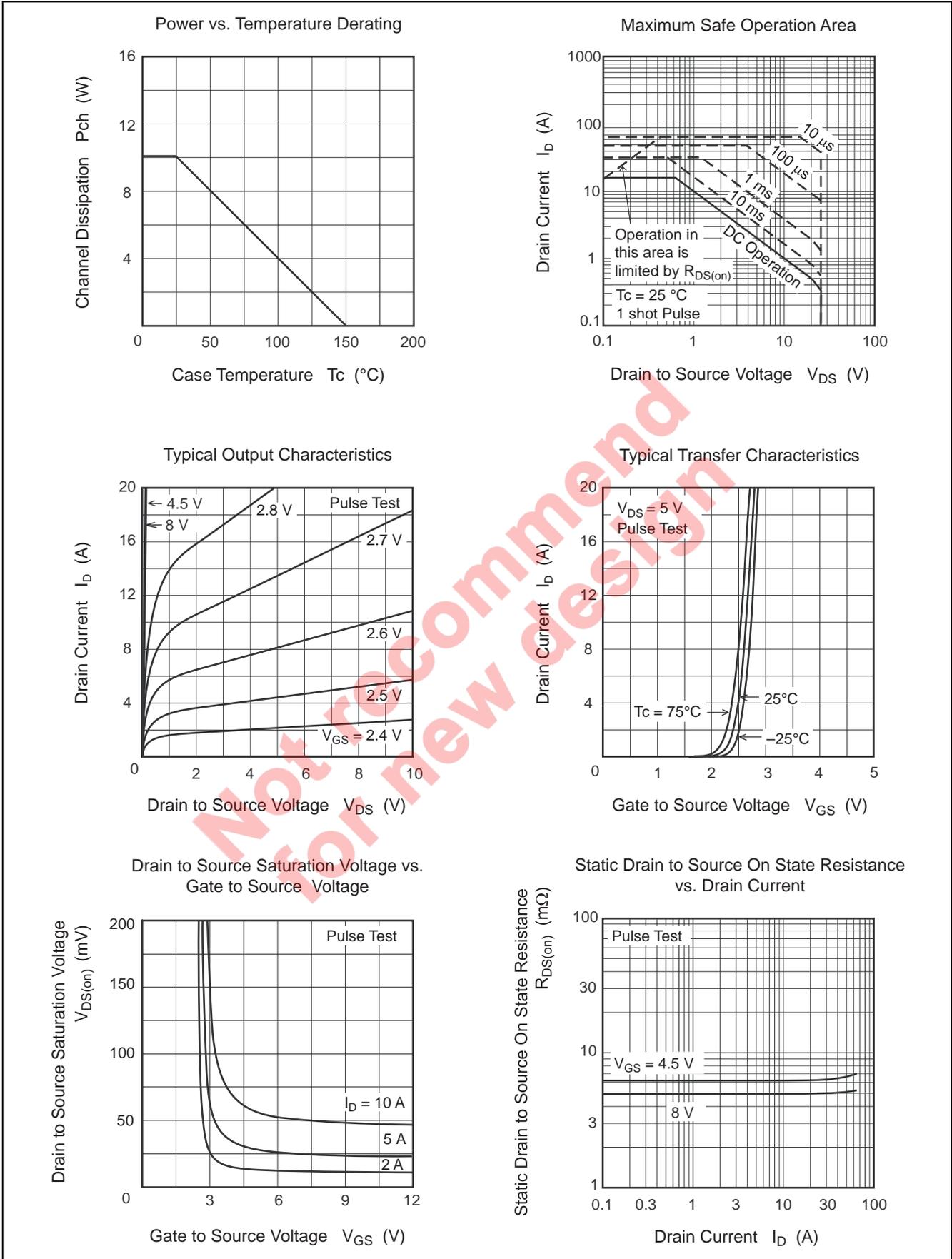
Switching Time Test Circuit



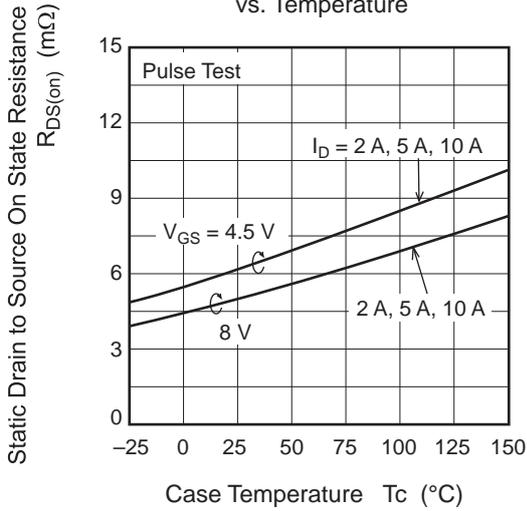
Switching Time Waveform



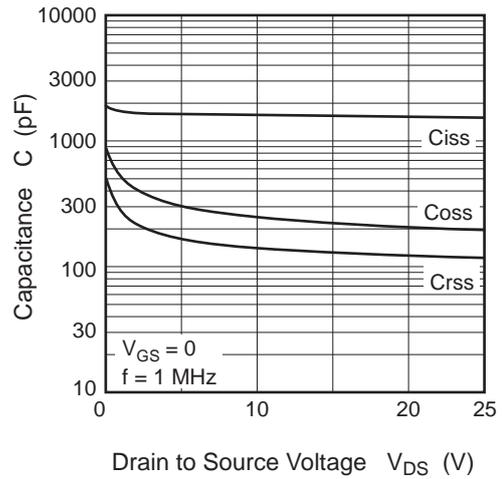
• MOS2 and Schottky Barrier Diode



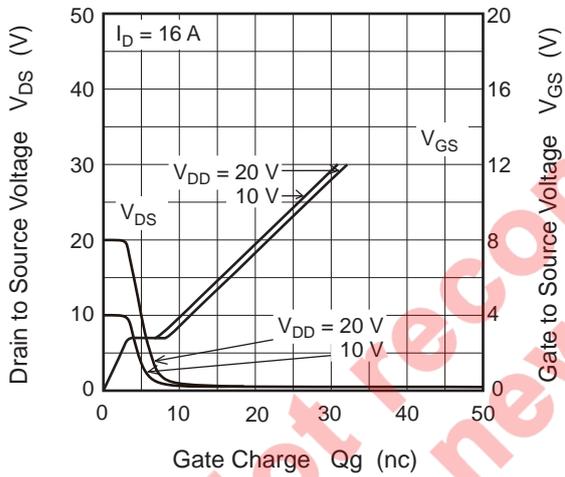
Static Drain to Source On State Resistance vs. Temperature



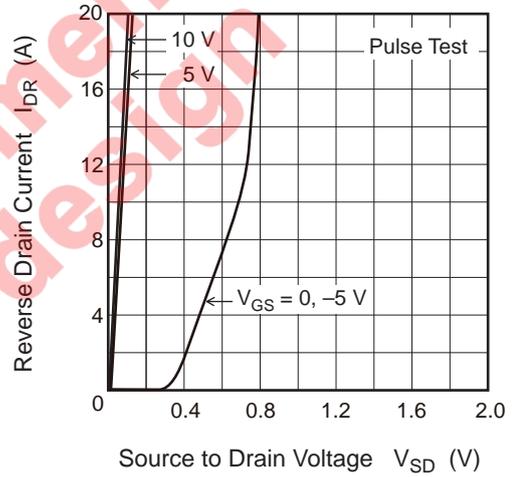
Typical Capacitance vs. Drain to Source Voltage



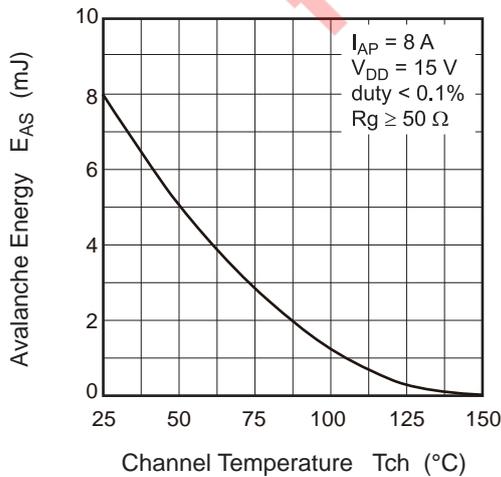
Dynamic Input Characteristics



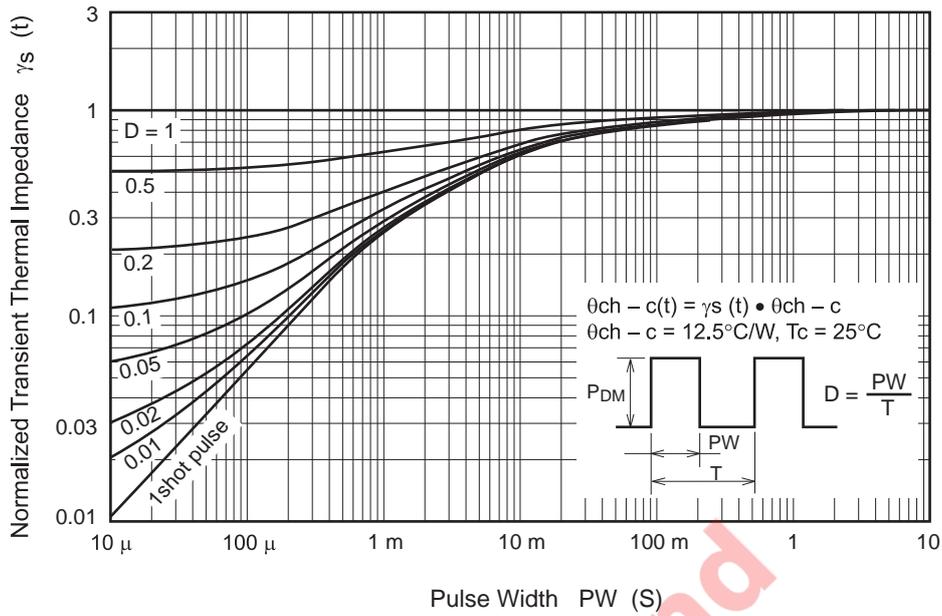
Reverse Drain Current vs. Source to Drain Voltage



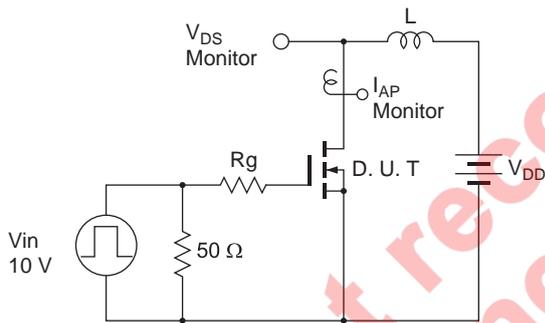
Maximum Avalanche Energy vs. Channel Temperature Derating



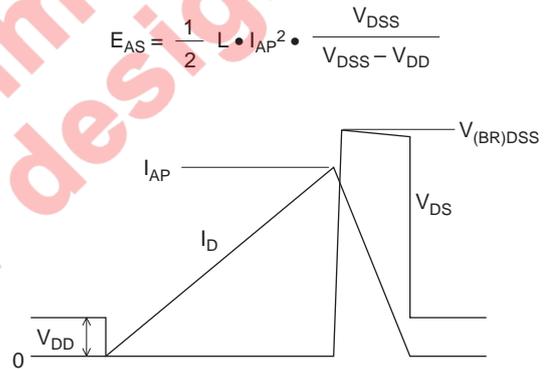
Normalized Transient Thermal Impedance vs. Pulse Width



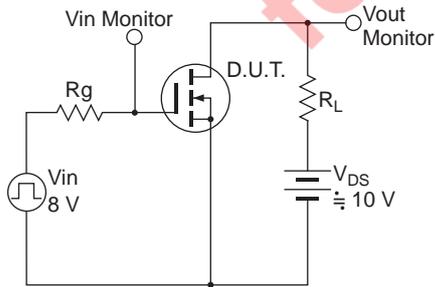
Avalanche Test Circuit



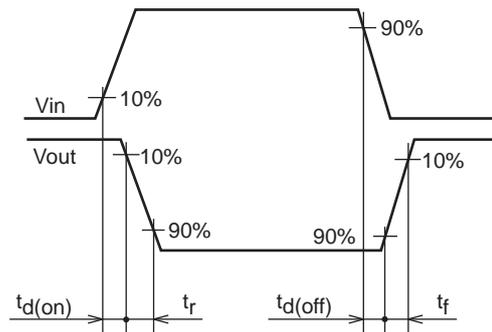
Avalanche Waveform



Switching Time Test Circuit



Switching Time Waveform





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