

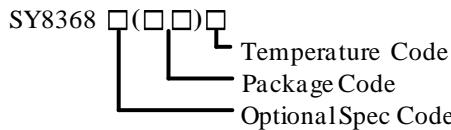
## High Efficiency Fast Response 8A Continuous, 16A Peak, 28V Input Synchronous Step Down Regulator

### General Description

The SY8368A develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 8A continuous, 16A peak current. The SY8368A operates over a wide input voltage range from 4.0V to 28V and integrates main switch and synchronous switch with very low  $R_{DS(ON)}$  to minimize the conduction loss.

The SY8368A adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 800kHz under continuous conduction mode to minimize the size of inductor and capacitor.

### Ordering Information



Ordering Number	Package type	Note
SY8368AQQC	QFN3x3-12	--

### Typical Applications

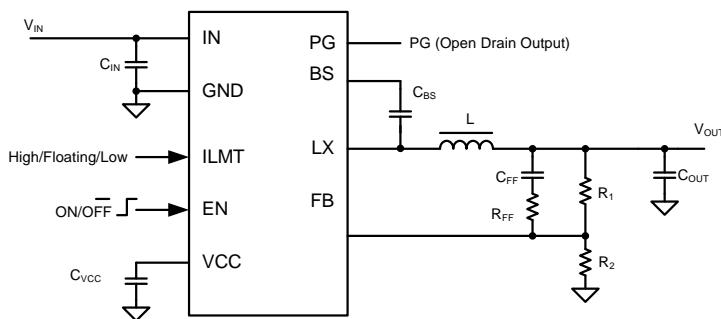


Figure 1 Schematic

### Features

- 4.0-28V Wide Input Voltage Range
- Low  $R_{DS(ON)}$  for Internal Switches: 20/10mΩ
- Instant PWM Architecture to Achieve Fast Transient Response
- Internal 600μs Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 800kHz
- 8A Continuous, 16A Peak Output Current Capability
- ±1% 0.6V Reference Voltage
- Hiccup Mode SCP, OVP
- Thermal Shutdown with Auto Recovery
- RoHS Compliant and Halogen Free

### Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

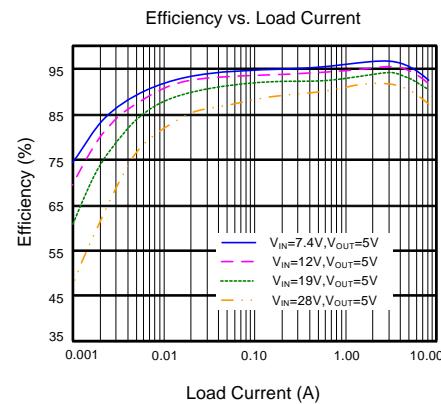
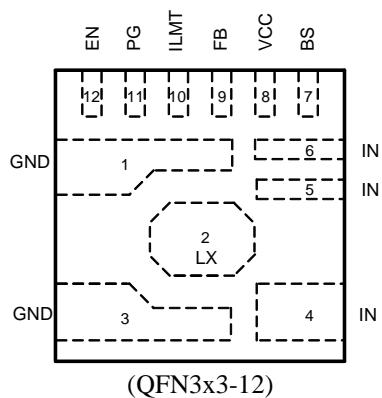


Figure 2. Efficiency

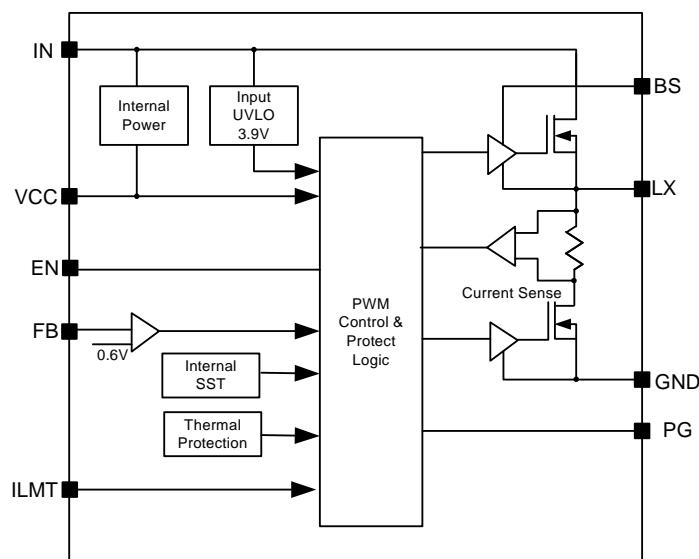
## Pinout (top view)



Top Mark: AVIxyz, (Device code: AVI, x=year code, y=week code, z= lot number code)

Pin Name	Pin Number	Pin Description
GND	1,3	Ground pin
LX	2	Inductor pin. Connect this pin to the switching node of inductor
IN	4,5,6	Input pin. Decouple this pin to the GND pin with at least a 10µF ceramic capacitor.
BS	7	Boot-strap pin. Supply high side gate driver. Decouple this pin to the LX pin with a 0.1µF ceramic capacitor.
VCC	8	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Bypass a capacitor to GND.
FB	9	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6 \times (1+R_1/R_2)$
ILMT	10	Current limit setting pin. The current limit is set to 8A, 12A or 16A when this pin is pulled low, floating or pulled high respectively.
PG	11	Power good Indicator. Open drain output when the output voltage is within 90% to 120% of regulation point.
EN	12	Enable control. Pull this pin high to turn on the IC. Do not leave this pin floating.

## Block Diagram



### Absolute Maximum Ratings (Note 1)

IN, LX, PG, EN	-0.3V to 30V
BS-LX, FB, ILMT, VCC	-0.3V to 4V
Power Dissipation, PD @ T <sub>A</sub> = 25 °C QFN3x3-12	3.3W
Package Thermal Resistance (Note 2)	
θ <sub>JA</sub>	30 °C/W
θ <sub>JC</sub>	4 °C/W
Junction Temperature Range	150 °C
Lead Temperature (Soldering, 10 sec.)	260 °C
Storage Temperature Range	-65 °C to 150 °C
Dynamic LX voltage in 50ns duration	IN+3V to GND-4V

### Recommended Operating Conditions (Note 3)

Supply Input Voltage	4V to 28V
Junction Temperature Range	-40 °C to 125 °C
Ambient Temperature Range	-40 °C to 85 °C

## Electrical Characteristics

(VIN = 12V, VOUT = 5V, COUT = 100uF, TA = 25 °C, IOUT = 2A unless otherwise specified)

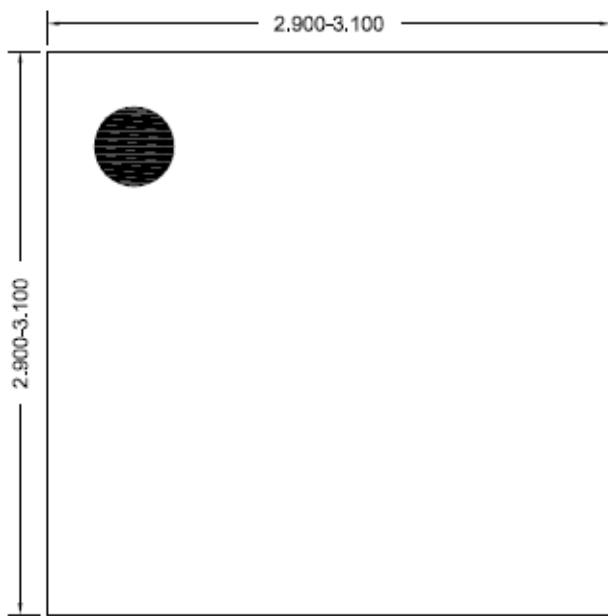
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V <sub>IN</sub>		4.0		28	V
Quiescent Current	I <sub>Q</sub>	I <sub>OUT</sub> =0, V <sub>FB</sub> =V <sub>REF</sub> ×105%		100		µA
Shutdown Current	I <sub>SHDN</sub>	EN=0		3	10	µA
Feedback Reference Voltage	V <sub>REF</sub>		0.594	0.6	0.606	V
FB Input Current	I <sub>FB</sub>	V <sub>FB</sub> =4V	-50		50	nA
Top FET RON	R <sub>DSON1</sub>			20		mΩ
Bottom FET RON	R <sub>DSON2</sub>			10		mΩ
Discharge FET RON	R <sub>DIS</sub>			50		Ω
Bottom FET Current Limit	I <sub>LIM</sub>	ILMT='0' ILMT=Floating ILMT='1'	8 12 16			A
ILMT Rising Threshold	V <sub>ILMTH</sub>		Vcc-0.8		V <sub>CC</sub>	V
ILMT Falling Threshold	V <sub>ILMLT</sub>				0.8	V
Soft Start Time	t <sub>SS</sub>			600		µs
EN Rising Threshold	V <sub>ENH</sub>		0.8			V
EN Falling Threshold	V <sub>ENL</sub>				0.4	V
Input UVLO Threshold	V <sub>UVLO</sub>				3.9	V
UVLO hysteresis	V <sub>HYS</sub>			0.3		V
Oscillator Frequency	F <sub>OSC</sub>	Vo=5V	0.68	0.8	0.92	MHz
Min ON Time	t <sub>ON,MIN</sub>	V <sub>IN</sub> =V <sub>INMAX</sub>		50		ns
Min OFF Time	t <sub>OFF,MIN</sub>			180		ns
VCC Output	V <sub>CC</sub>	V <sub>IN</sub> =4.2V	3.2	3.3	3.4	V
Output Over Voltage Threshold		V <sub>FB</sub> rising	115	120	125	%V <sub>REF</sub>
Output Over Voltage Hysteresis				2		%V <sub>REF</sub>
Output Over Voltage Delay Time				20		µs
Power Good Threshold		V <sub>FB</sub> rising (Good)	88	90	92	%V <sub>REF</sub>
Power Good Hysteresis				2		%V <sub>REF</sub>
Power Good Delay Time				10		µs
Thermal Shutdown Temperature	T <sub>SD</sub>			150		°C
Thermal Shutdown hysteresis	THYS			15		°C

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

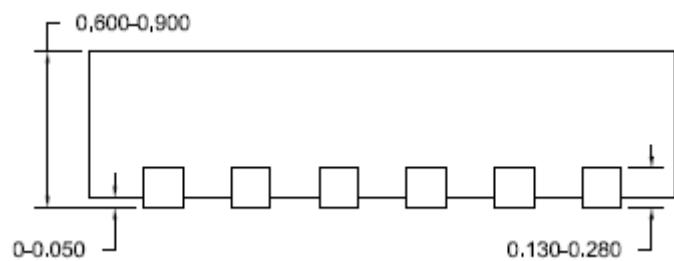
**Note 2:** θ<sub>JA</sub> is measured in the natural convection at T<sub>A</sub> = 25 °C on a four-layer Silergy Evaluation Board.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

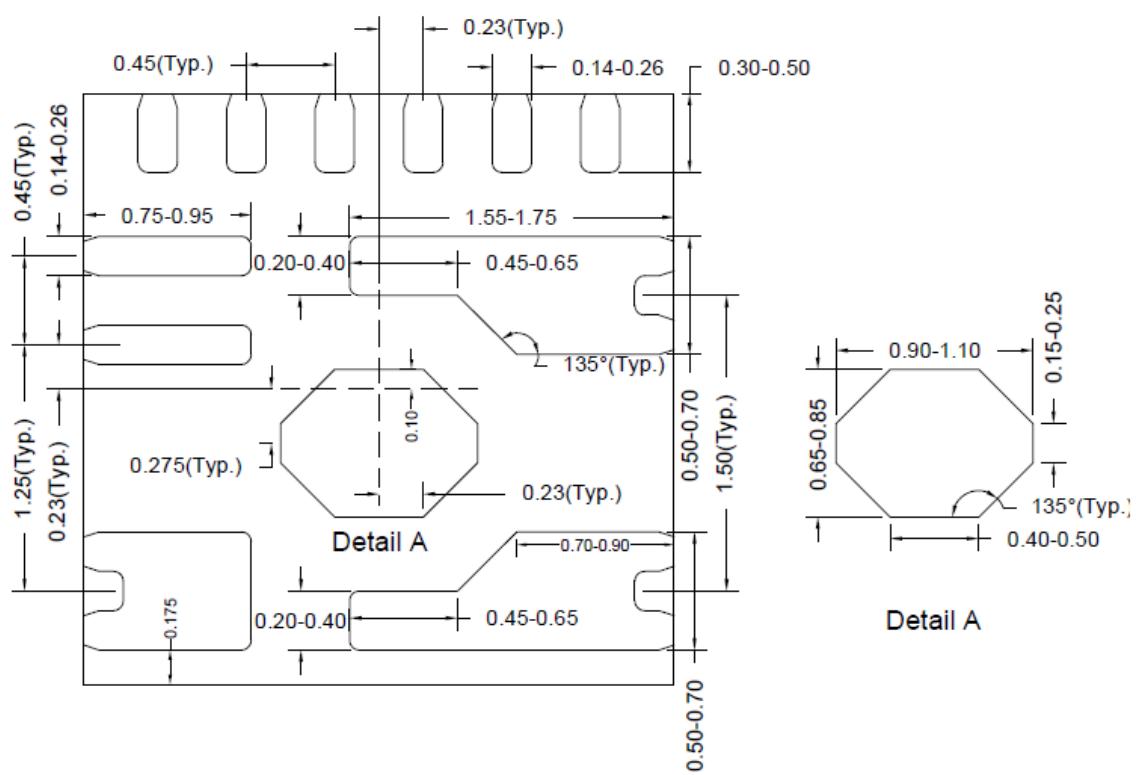
### **QFN3x3-12 Package Outline Drawing**



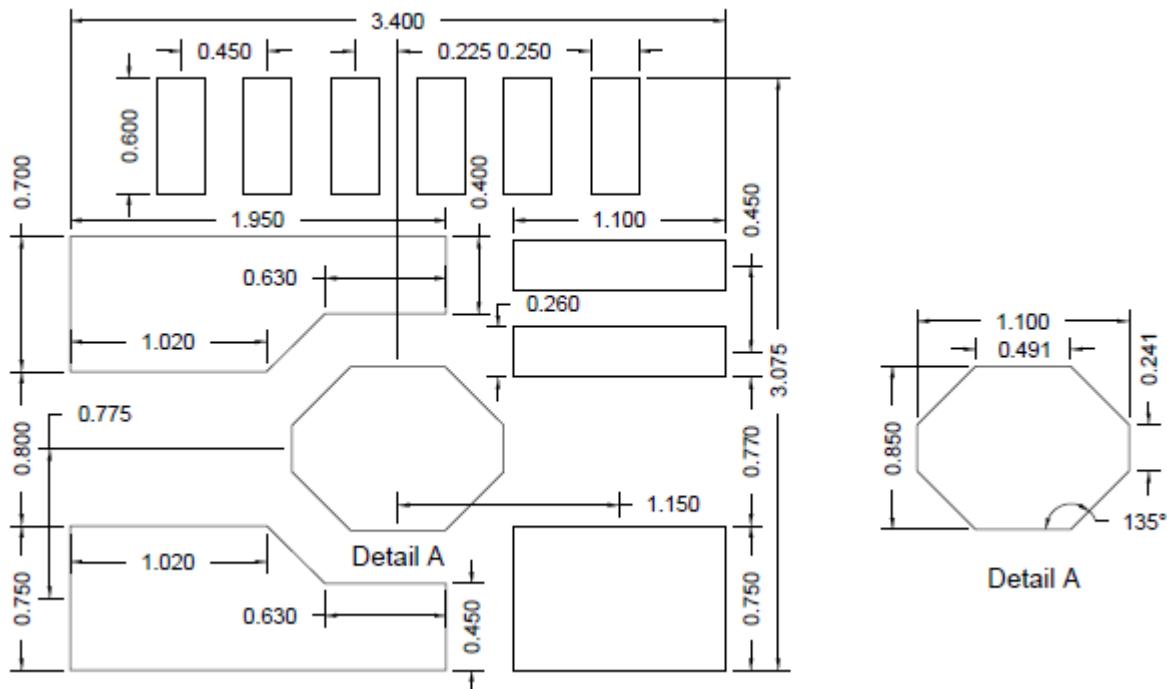
**Top View**



**Side View**



**Bottom View**



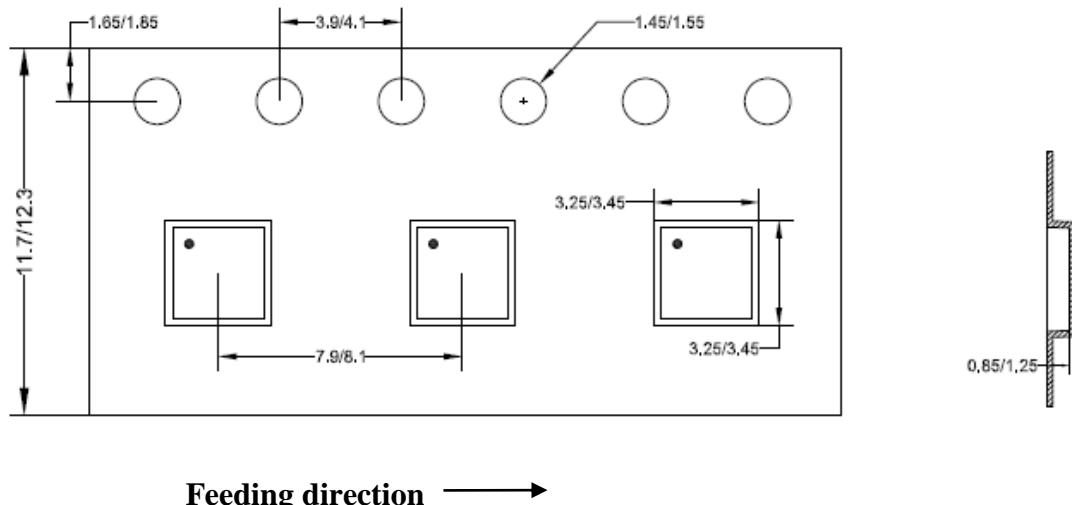
**Recommended PCB layout  
(Reference Only)**

**Notes:** All dimension in MM and exclude mold flash & metal burr.

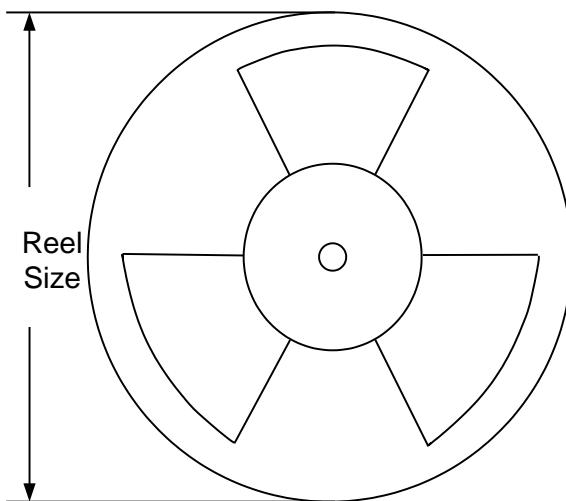
## Taping & Reel Specification

### 1. Taping orientation

QFN3x3



### 2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x3	12	8	13"	400	400	5000

### 3. Others: NA